AMENDMENT TO THE CLAIMS

Claim 1 (Original) An erasable programmable read only memory that omits a control gate comprising:

a doped region formed by ion implantation in a substrate;

a first conductive area covered on said substrate and forms a first cross structure with a first overlap area to acts as a select transistor gate and connected to a select gate voltage (V_{SG});

a second conductive region located at a side of said first conductive region and on said substrate and forms a second cross structure with a second overlap area to acts as a floating gate;

wherein a feature of said erasable programmable read only memory is that a control gate is omitted, thereby reducing device size and integratable with CMOS process.

2 (Original) The erasable programmable read only memory of Claim 1 wherein during a mode for writing "digital one", a selected word line is grounded and a unselected word line is bias to about a first voltage, wherein a selected bit line is grounded, a unselected bit line is about said first voltage, a source node and a N well are connected to said first voltage, thereby turning on said selected transistor and injecting hot channel carrier onto said floating gate of said second P-type metal-oxide semiconductor transistor.

3 (Original) The erasable programmable read only memory of Claim 1 wherein during a mode for writing "digital zero", a selected word line is grounded and a unselect word line is applied to a second voltages, a selected bit line is about said first second voltage and a unselect bit line is also about said second voltage, a source node and a N well are respectively connected to said second voltage, thereby turning off said select transistor and hot carrier is unable to inject onto said floating gate.

4 (Original) The erasable programmable read only memory of Claim 1 wherein during read mode, a selected word line is grounded and unselected word line is biased to a third voltages, a selected bit line is about a forth voltage, a unselect bit line is biased to

said third voltage, a source node is also bias to said third voltage and a N well is connected to said third voltage, thereby turning on said select transistor for reading the status stored in said floating gate.

5 (Original) The erasable programmable read only memory of Claim 1 wherein a cell array, an unselect transistor does not suffer a drain disturbance because said unselect transistor is at off-state and the electric field between said bit line and said floating gate is not strong enough to inject/generate hot carriers, a coupling of said floating gate is not induced by the word line, thereby eliminating the gate disturbance phenomenon.

Claims 6-8 (Canceled)